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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,706	07/31/2003	Yoshiro Mikami	500.41297CX1	1602

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EXAMINER	
LIANG, REGINA	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,706	MIKAMI ET AL.	
	Examiner	Art Unit	
	Regina Liang	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to amendment filed 2/21/06. Claims 1-14 are pending in this application.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

3. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Komiya (US. PAT. NO. 6,509,692).

As to claim 1, Figs. 1 and 7 of Komiya discloses an image display apparatus comprising: a plurality of scanning wires (gate lines 1); a plurality of signal wires (data line 2); a plurality of current driven electro-optical display elements (organic EL 7) each arranged in a pixel region surrounded by the scanning wires and the signal wires connected to a common power supply (driving lines 3 is connected to a power source PV); a plurality of driving elements (driving TFT 6) arranged in the pixel region connected with the display elements (organic EL 7). Komiya also discloses the apparatus having a plurality of memory control circuits (selection transistors 4 and storage capacitor 5 corresponding memory control circuits) for holding the signal voltage in response to the scanning signal to control driving of the driving elements based on the held signal voltage, and the memory control circuit samples and holds the signal voltage while blocking a bias voltage from being applied to each of the driving elements, and subsequently applies the driving elements with the held signal voltage as the bias voltage (referring to Fig. 1 for example, in response to the scanning signal on gate line 1, selection transistors 4 are closed with the driving transistor 6 left opened so that a signal voltage from the data line 2 is applied to

the storage capacitor 5 through the selection transistors 4, and charged and held on the storage capacitor 5, see col. 1, line 47 to col. 2, lines 12 for example).

As to claim 2, Komiya teaches the driving lines 3 is connected to a power source PV for supplying or stop supplying the power to the driving elements.

As to claim 3, Komiya teaches the memory control circuit (selection transistors 4 and storage capacitor 5) comprises a main driving switch element (4a) responsive to the scanning signal for scanning line (1) to conduct for sampling the signal voltage, and a sampling capacitor (storage capacitor 5) for holding the signal voltage sampled by the main sampling switch element.

As to claim 4, Komiya teaches the memory control circuit (selection transistors 4 and storage capacitor 5) comprises a main driving switch element (4a) responsive to the scanning signal (from scanning line 1) to conduct for sampling the signal voltage, and a sampling capacitor (storage capacitor 5) for holding the signal voltage sampled by the main sampling switch element, an auxiliary driving switch element (4b) responsive to the scanning signal (from scanning line 1) to conduct for connecting one end of the sampling capacitor (5) to a common electrode).

As to claim 5, Komiya teaches the current driven electro-optical display elements comprising organic LEDs.

As to claim 6, note the discussion of claim 1 above. In addition, Komiya (Fig. 1 for example) teaches when selection transistors 4 are closed with the driving transistor 6 left opened so that a signal voltage from the data line 2 is applied to the storage capacitor 5 through the selection transistors 4, and charged and held on the storage capacitor 5, this corresponds to a

voltage applied to the driving elements in a sampling period, in this period, no voltage is applied to the driving element. Komiya also teaches when the driving transistor 6 is closed, the signal voltage held on the capacitor is applied to the driving transistor 6, this corresponds to the voltage applied to the driving elements in a write period. Thus, Komiya teaches the voltage applied to the driving elements in a sampling period is lower than a voltage in a write period.

As to claim 7, Komiya teaches when selection transistors 4 are closed with the driving transistor 6 left opened so that a signal voltage from the data line 2 is applied to the storage capacitor 5 through the selection transistors 4, and charged and held on the storage capacitor 5, this corresponds to the driving elements (driving transistor 6) are non-conductive in a sampling period.

As to claim 8, Komiya teaches the memory control circuit (selection transistors 4 and storage capacitor 5) comprises a main driving switch element (4a) responsive to the scanning signal (from scanning line 1) to conduct for sampling the signal voltage, and a sampling capacitor (storage capacitor 5) for holding the signal voltage sampled by the main sampling switch element.

As to claim 9, Komiya teaches the memory control circuit (selection transistors 4 and storage capacitor 5) comprises a main driving switch element (4a) responsive to the scanning signal (from scanning line 1) to conduct for sampling the signal voltage, and a sampling capacitor (storage capacitor 5) for holding the signal voltage sampled by the main sampling switch element, an auxiliary driving switch element (4b) responsive to the scanning signal (from scanning line 1) to conduct for connecting one end of the sampling capacitor (5) to a common electrode.

As to claim 10, Komiya teaches the current driven electro-optical display elements comprising organic LEDs.

As to claim11, note the discussion of claim 1 above. In addition, Komiya (Fig. 1 for example) teaches when selection transistors 4 are closed with the driving transistor 6 left opened so that a signal voltage from the data line 2 is applied to the storage capacitor 5 through the selection transistors 4, and charged and held on the storage capacitor 5, this corresponds to a voltage applied to the driving elements in a sampling period, in this period, no electric power is applied to the driving element since the driving transistors 6 are opened. Komiya also teaches when the driving transistor 6 is closed, the signal voltage held on the capacitor is applied to the driving transistor, this corresponds to the voltage applied to the driving elements in a write period, in this period, the electric power are supplied to the driving elements since the driving transistors 6 are closed. Thus, Komiya teaches the electric power supplied to the driving elements (transistor 6) in a sampling period is lower than the electric power in a write period.

As to claim 12, Komiya teaches the memory control circuit (selection transistors 4 and storage capacitor 5) comprises a main driving switch element (4a) responsive to the scanning signal (from scanning line 1) to conduct for sampling the signal voltage, and a sampling capacitor (storage capacitor 5) for holding the signal voltage sampled by the main sampling switch element.

As to claim 13, Komiya teaches the memory control circuit (selection transistors 4 and storage capacitor 5) comprises a main driving switch element (4a) responsive to the scanning signal (from scanning line 1) to conduct for sampling the signal voltage, and a sampling capacitor (storage capacitor 5) for holding the signal voltage sampled by the main sampling

switch element, an auxiliary driving switch element (4b) responsive to the scanning signal (from scanning line 1) to conduct for connecting one end of the sampling capacitor (5) to a common electrode.

As to claim 14, Komiya teaches the current driven electro-optical display elements comprising organic LEDs.

Response to Arguments

4. Applicant's arguments filed 2/21/06 have been fully considered but they are not persuasive.

Applicant's remarks regarding claim 1 in that "Komiya does not appear to disclose a display device wherein the memory control circuits sample and hold the signal voltage while blocking a bias voltage from being applied" on page 10 are not persuasive.

Figs. 1 and 7 of Komiya teaches when the gate signal is turned on, the transistors 4 connected that gate line 1 are turned on, in the data line 2, a data signal determined in accordance with a displayed image is applied from a data line 2, and is therefor applied to the gate of the driving transistor 6 and charged in the storage capacitor 5, this corresponds to the memory control circuit samples and holds the signal voltage and this period corresponds to a sampling period. Komiya also teaches the driving transistor 6 connecting the driving line 3 and the OEL 7 at an electrical conductivity corresponding to the value of the data signal, the data signal is supplied to the gate electrode, and the gate voltage VG of transistor 6 is a value corresponding to the data signal.

As shown in Figs. 5 and 9, the gate voltage VG of driving transistor 6 has to reach VG_{min} to turn on the driving transistor 6, before the gate voltage VG reaches the VG_{min}, the driving

transistor 6 is turned off, therefore, by the time when charging the storage capacitor 5 (memory control circuit samples and holds the signal voltage), the driving transistor 6 is turned off, no voltage from being applied to the OEL 7, this corresponds memory control circuit samples and holds the signal voltage while blocking a bias voltage from being applied to each of the driving elements as claimed. When the gate voltage VG of the driving transistor 6 reaches VG_{min}, the driving transistor 6 is turned on, a current corresponding to the data signal is supplied from driving line 3 to OEL 7 through the driving transistor 6, this corresponds to subsequently applies driving elements with the held signal voltage as bias voltage and this period corresponds to a write period.

Applicant's remarks regarding claims 6 and 11 on page 11-14 are not persuasive. As stated above, the gate voltage VG of driving transistor 6 has to reach VG_{min} to turn on the driving transistor 6, before the gate voltage VG reaches the VG_{min}, the driving transistor 6 is turned off, the memory control circuit is sampling and holding the signal voltage, this period corresponds to a sampling period. After the gate voltage VG of driving transistor 6 reaches VG_{min} to turn on the driving transistor 6, a current corresponding to the data signal is supplied from driving line 3 to OEL 7 through the driving transistor 6, this period corresponds to write period. See Fig. 5 for example, a voltage in a sample period ($VG < VG_{min}$) is lower than a voltage in a write period ($VG_{min} < VG < VG_{max}$).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (571) 272-7693. The examiner can normally be reached on Monday-Friday from 8AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Regina Liang
Primary Examiner
Art Unit 2674

3/31/06